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HOST CONTROL INTERFACE AND REGISTERS AIDED CONTINUOUSLY PROGRAMMABLE FIR FILTER DESIGN FOR NON-LINEAR DSP APPLICATIONS

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ABSTRACT

This paper aims to design a continuously programmable digital finite impulse response(CPDF FIR) filter for non-linear signal filtering resolutions. The proposed CPDF FIR filter encompasses input block, host-control interface (HCI), register blocks aided parallel filter module, and an output block. The inputincepts with non-linear sequentially repeating chirp signal, which is subsequently processed for frame based (floating to fixed) sample generation and delay insertion. Here one sample per frame is used to avoid sample overflow and quantization error with the introduction of one clock delay. Consequently, the delayed sampled signal was subsequently processed using register block which functions in unification with HCI. Here, HCI helps in coefficient updates as well as low-pass coefficient assignment to the Butterworth direct discrete FIR filter for reference signal generation. On the other hand, it helps continuous coefficient update to the register block. Prominently, the register block uses low pass coefficients to filter each chirp signal or delayed samples in the beginning, followed by high-pass filter coefficient using direct discrete FIR filter model. CPDF with linear and differential optimization approach are used for coefficient updates. The overall work exposes that the proposed CPDF FIR filter accomplishes optimal filtering performance with low area, minimum hardware consumption such as reduced multipliers(43) and adder/subtractors(42). Furthermore, it exhibits significantly low delay of 6.166 ns. Such robustness indicates suitability of the CPDF-FIR filter towards varied non-linear filtering applications including industrial IoT data filtering or speech signals.

KEYWORDS: *Continuously programmable digital filter, fir filter, host control interface, delay insertion, parallel fir, multiplier reduction*

INTRODUCTION

The augmented rise in skills and allied applications have widened perspective for different demands pertaining to digital communication, transmission systems, internet of things (IoT), industrial communication and varied decision systems. The two significant filter technologies are the analog filters and the digital filters [1]. Nevertheless, analog filters are low-cost, rapid and possess dynamic range in both amplitude and frequency;

digital filters govern the industry rather due to its superior performance[1-3]. The advent of digital signal processing (DSP) technologies has widened the skyline for digital filters over conventional analog filters[1].The

design complexity and higher order demand of major digital filters have remained challenge for industry[1]. Furthermore, its efficacy as the anti-aliasing filter too has remained confined, nevertheless numerous designs have been proposed such as Finite Impulse Response (FIR) filters and the Infinite Impulse Response (IIR) filters. FIR filters are relatively easier to design; though constraints such as higher hardware complexity and increased order of design cause power and area exhaustion. Such constraints limit its employability in real-world miniaturized application environment. Interestingly, the ability of FIR filter to achieve linear phase characteristics with symmetric coefficient makes it applicable in numerous applications. Architecturally, IIR filters are relatively more complex to design; however its efficacy dominates over the classical FIR filters[3].

The flexibility, ease of design, reliability and scalability of FIR filters make it suitable for real-world DSP applications. Majority of the existing filter designs are time-invariant signifying "design with fixed coefficients". However, to cope up with non-linear systems it requires adopting varying or continuously programmable (say, signal adaptive) coefficient information. To achieve it, digital filters with programmable coefficient can be of great significance, especially to adapt time-varying systems. Such filter designs with programme based coefficient update are often stated as continuously programmable digital filters (CPDF). Though, a few researches have been done towards FIR design; however very less effort is made for CPDF FIR filter design, which does have superior performance and employability. This work emphasis on designing CPDF FIR filter with continuous programmable coefficients by using host control interface(HCI) and register block, which strategically enables dynamic coefficient, update to perform non-linear data filtering without imposing huge hardware utilization or area demands.

System Model

FIR filter design constraints, CPDF FIR design optimization and its implementation for speech signal filtering etc. are discussed below.

Fir Filter Design Constraints

FIR filters are designed based on certain routines or the algorithms specifically by employing difference equations in varied forms like cascade design, parallel, ladder or others[5][6]. These designs apply a common difference equation, given as(1)

$$\sum_{n=0}^{N} d_n y(k-n) = \sum_{m=0}^{M} c_m x(k-m) \quad (1)$$

The above derived difference equation(1) retrieves the output $y(k)$ for different instants of$k = 0,1,2, \ldots$ by employing an iterative function (2). Here,N represents the total number of samples.Equation (1) can further be derived as(2).

$$y(k-n) = \frac{1}{d_0}\{\sum_{m=0}^{M} c_m x(k-m) - \sum_{n=1}^{N} d_n x(k-m)\} \quad (2)$$

Majority of the classical FIR filters are time-invariant signifying fixed coefficient values(c_m andd_n). However, it limits its efficiency for non-linear filter demands. To cope up with non-linear systems and IoT signals, which can often exhibit non-linear behave and abrupt changes, it becomes vital to enhance conventional FIR filter designs. To achieve it, dynamically updating or tuning filter coefficient is more significant. However,

doing so can be cost-consuming and therefore it is vital to design a cost-efficient(i.e., low hardware utilization, low power and delay) FIR filter with continuously programmable coefficient tuning is a must. In this work, a CPDF FIR design is proposed using optimally designed host control interface(HCI) and register blocks, which helps in continuously updating the coefficient based on signal inputs to accommodate non-linear signal filtering. The proposed HCI and register block based filter incorporates the algorithm which estimates, validates and updates filter-coefficients dynamically with time(so as to adopt time-varying non-linear systems such as digital system compensator, adaptive filters, noise filters or compensator, etc).

This work proposes a robust CPDF FIR filter design, which intends to retain higher efficiency with low computational cost, power and area exhaustion. Furthermore, it intends to maintain low computation time to ensure real-world applicability.

Continuously Programmable Digital Filter Optimization

Practically, retrieving$H(z)$ from$H(s)$ using bilinear transformation method can be hypothesized to be the same as derived from the model called Simpson's Rule approximation difference equation. It resembles differential equation signifying a form of$H(s)$. Although, $H(s)$ in FIR filter can be defined merely for the linear time-invariant models, other non-linear or time-varying models too can be approximated iteratively by means of transform relationship. Such approximation helps in coefficient(a_n andb_m) estimation and continuous update. It becomes feasible as the transformation method involved is equivalent to the time-domain process. Following this concept, to design CPDF FIR filter, we need to generate the coefficients d_n and c_m for $D(N)$ and $N(z)$, respectively. Mathematically, these functions are presented as (3) and (4).

$$H(z) \triangleq \frac{\sum_{m=0}^{M} b_m s^m}{\sum_{n=0}^{N} a_m s^n} \tag{3}$$

Provided, $s = \frac{z-1}{z+1}$

It can further be derived as (4).

$$H(z) = \frac{\sum_{0}^{M} b_m (z-1)^m (z+1)^{N-m}}{\sum_{0}^{N} a_n (z-1)^n (z+1)^{N-n}} \triangleq \frac{N(z)}{D(z)} \tag{4}$$

In(4),$2/T$ is hypothesized to be unit value 1 with no loss of generality. This is because the scale factor$2/T$ in the bilinear transformation can easily be handled using(5).

$$b_m \leftarrow \left(2/T\right)^m b_m, \text{ and } a_n \leftarrow \left(2/T\right)^n a_n \tag{5}$$

CPDF FIR Implementation for Audio Signal Filtering

The proposed CPDF FIR filter$H(z)$ is derived from analog$H(s)$ prototype models while ensuring that it fulfills the frequency domain criteria in z-domain. To achieve it, optimization has been done over the s-domain coefficients. Here, CPDF FIR optimization takes place with the initial step of$H(s)$ prototype approximation which helps in identifying a targeted error or cost function$H(z)$ criteria in the frequency domain. Subsequently, coefficient update mechanism is executed to obtain$H(z)$ and consequent$H(z)$ frequency response. In the proposed

model, HCI helps in assigning low-pass coefficient to the Butterworth filter, while same helps updating the high-pass coefficient to the register block, which employs parallel discrete FIR filter design to perform filtering over all input samples. Noticeably, HCI and register blocks are designed in such manner(Fig. 1), that it avoids any additional chip and therefore is hardware efficient. As micro-level characterization, register block employs coefficient register and shadow register to perform high-pass coefficient update to accommodate non-linear input signal's filtering.

Hardware Implementation

Our proposed CPDF FIR model encompasses four key modules. These are (Fig. 1):

- *Input and Delay Insertion Modules,*
- *Host Control Interface,*
- *Register Block and Parallel Filter Architecture, and*
- *Output Block.*

It has been implemented as parallel-designed bank-of filters, where each filter possesses varied filter-response on the chip.

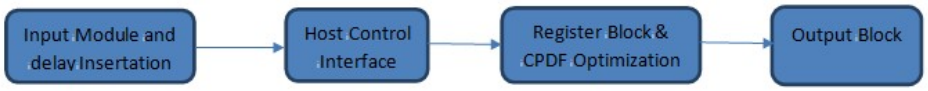

Figure 1: Proposed CPDF FIR Filter Architecture.

Input Modules and Delay Insertion

As depicted in Fig. 1, CPDF FIR filter incepts with the input of a non-linear chirp signal, which is further processed with fixed point conversion and delay insertion before filtering. It has three components, input original signal($H(s)$, fixed point converter and delay insertion module. Considering signal non-linearity and variation, we considered non-linear chirp signal as input with the start frequency of 1 Hz and end frequency of 500 Hz(additionally we tested it with the maximum frequency of 4 KHz) to be filtered. To introduce non-linearity with the input, we applied repeating(sequence) chirp Signal(RCS) in which the frequency response varies throughout samples. The generated input signals also called input signal matrix characterizes one channel per column, where signal columns were buffered into frames. To avoid overflow or abrupt flooding problems we introduced delay insertion module which inserted a delay of a few clocks throughout the signal.

Host control Interface (HCI)

In the proposed CPDF FIR design(Fig. 1), HCI executes dual-tasks; first to update Butterworth FIR filter with low pass coefficient, and second to update register block continuously with updated high-pass coefficients for further optimization. Structurally(Fig.1), HCI possesses four key functions $Host\_w\_DATA$,$Host\_w\_ADDRES$,$Host\_w\_ENABLE$ and$Host_w_DONE$. Simultaneously, with updated low pass coefficient values with$Host_w_ENABLE$ and$Host_w_DONE$ as high(or 1), it updates CPDF FIR register block, which subsequently estimates the shadow coefficient to be further updated as input(high-pass) coefficient

for the discrete FIR filter for final chirp sample filtering. Functionally, the low pass coefficients are updated to the discrete FIR filter only when write enable$Host_w_ENABLE$ and write DONE$Host_w_DONE$ are high or 1.

Register Block and Parallel Filter Architecture

As discussed in the previous section, in FIR filter, the filter-coefficients of the two distinct$s$-domain are defined. Thus, with reference to the updated coefficients, our proposed CPDF FIR filter model filters non-linear inputs and the above stated process continues till the complete input signal is processed.

Output Block

The output block signifies a conjunction where different inputs containing original input data$H(s)$, reference signal, error data etc are presented altogether. As depicted in Fig. 1, our proposed model encompasses reference direct FIR filter based output signal(say, reference signal), CPDF FIR filtered output signal, error, enable port with respect to which the outputs have been obtained. These output points signifies efficiency of the proposed CPDF FIR filter to achieve maximum filter-efficiency with zero error.

RESULTS AND DISCUSSIONS

In this paper the predominant emphasis was made on designing a low-cost and computationally efficient discrete FIR filter design model, which could cope up with non-linear signals filtering demands. We considered chirp speech signal as input for filter performance assessment. As design solution, we focused on developing a continuous programmable digital filter solution with two key enhancement units, Host Control Interface(HCI) and register blocks based parallel filter module. Here, the overall proposed model can be visualized to be designed over single chip, due to efficient interface of HCI which updates coefficients across the parallel structure. To assess performance of the proposed model, we obtained simulated outcomes in terms of original signals, filtered signals, error performance etc. Additionally, we examined it for hardware utilization as well. The overall simulation was done using MATLAB 2019b and FPGA HDL plug in available with SIMULINK tool.

Table 1: Code-Interface Specification

Input Ports		
Port Name	**Data Type**	**Bits**
Clk	Boolean	1
Reset	Boolean	1
Clk_Enable	Boolean	1
Coeff_IN	sfix14_En13	14
Write_ADDRESS	unit8	8
Write_ENABLE	Boolean	1
Write_DONE	Boolean	1
Filter_IN	sfix14_En13	14
Output Ports		
Ce_OUT	Boolean	1
Filter_OUT	sfix14_En13	15

The generic resource report for the hardware utilization is given in Table 2.

Table 2: Hardware Utilization Report

Component	Specifications	Numbers
Multipliers	14 × 14 bit Multiply	43
Adders/Subtractors	31 × 31 bit Adder(1) 31 × 31 bit(41)	42
Registers	14-bit registers	128
Total 1-bit registers	-	1792
RAMs	-	0
Multiplexers	14-bit 2-to-1 Multiplexer(43) 29-bit 3-to-1 Multiplexer(43) 31-bit 3-to-1 Multiplexer(41)	127
I/O bits	[+] No. of Input bits: 41 [+] No. of Output bits: 16	57
Static Shift Operators	-	0
Dynamic Shift Operators	-	0

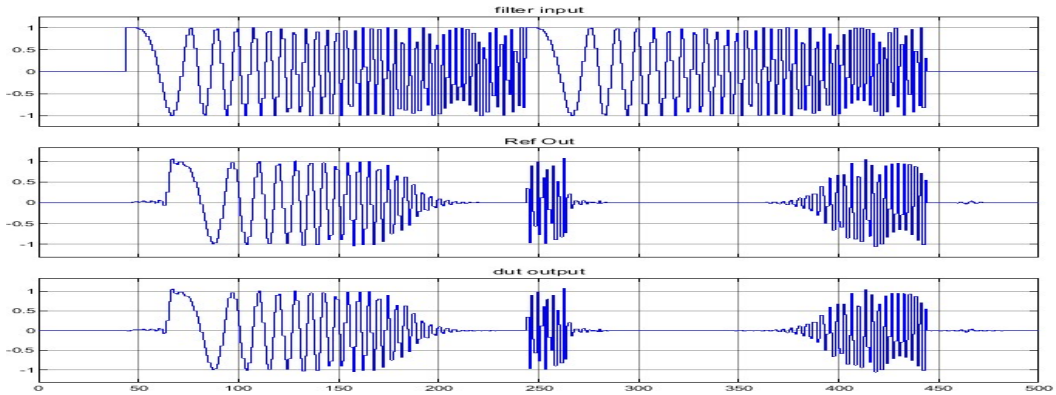

Figure 2: Simulated Results For theFilter_INPUT signal, Ref_OUT signal and DUT filtered Signal (x-axis represents time[samples], while y-axis signifies the amplitude)

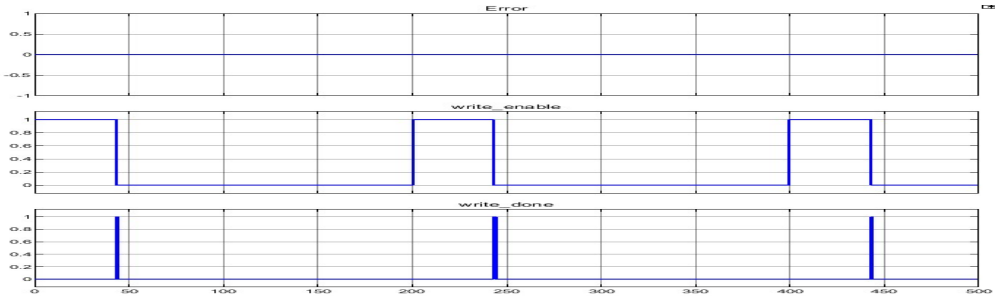

Figure 3: Simulated Results For the Error Performance

(i.e., difference between Ref_OUT signal and DUT (CPDF FIR filter) filtered signal) and signals statusThe $Write\_ENABLE$ and $Write\_DONE$ clock(say, edge) status over different instants and corresponding filtered(signal) output are given in Fig. 3. Logic analyser based outputs are depicted in Fig. 4.

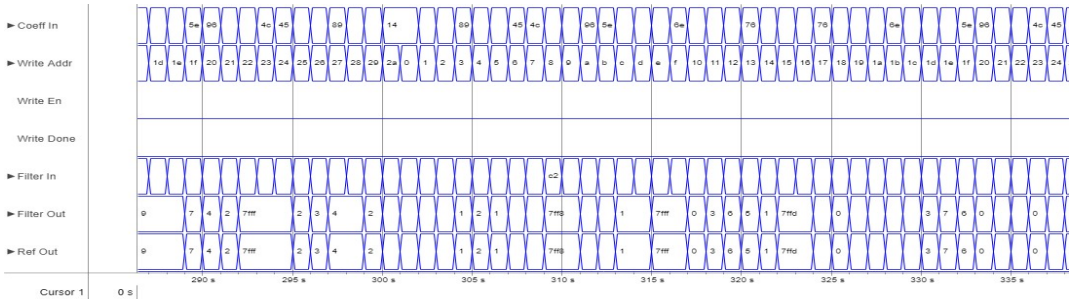

Figure 4: Logic Analyser Based Signal Processing Assessment

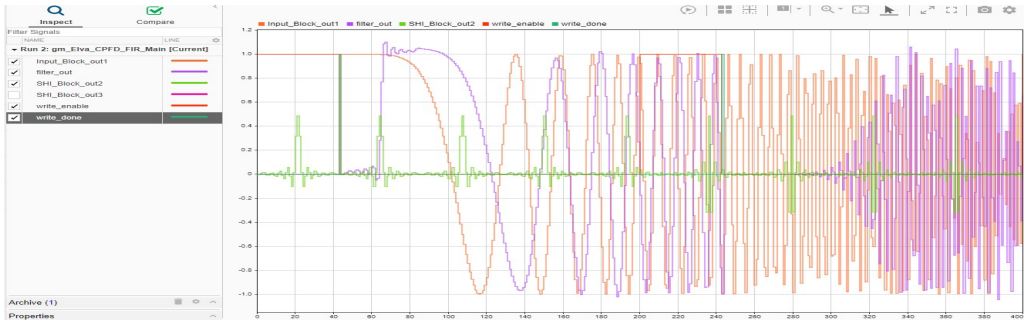

Figure 5: Data inspection performanceFig. 5 presents the data inspection output for the complete developed model and allied simulation.

CONCLUSIONS

Considering the significance of robust non-linear filters for non-linear signal filter purposes, in this paper the emphasis was made on developing a novel continuous programmable digital filter. To meet major filtering demands FIR filters have been found more efficient for those applications possessing linear phase characteristics. The proposed system was designed in such manner that it could accommodate or provide filtering solution to both non-linear systems as well as the signals demanding linear or non-linear phase demands such as speech signal. More specifically, the proposed model was assessed with speech (non-linear) signal. The overall proposed CPDF filter was designed as a parallel direct discrete FIR filter, where a supplementary host interface was designed to load low-pass coefficient to the Butterworth filter. Thus, the inclusion of HCI and register block with CPDF enabled dynamic or adaptive coefficient update to the FIR filter, which is continued till all samples are processed or filtered. One of the key novelties of this work is that it was developed on a single chip structure which reduced area and power consumption. The proposed CPDF FIR filter achieves optimal filtering accuracy with low area, power and delay. The implementation of HCI unit enabled coefficient update simultaneously to the low-pass Butterworth filter as well as register blocks for CPDF based optimization. Simultaneously, in CPDF optimization, the input delayed samples(chirp signal) was processed with low-pass coefficients which was succeeded with high pass coefficient update though shadow register. The simulation results affirmed zero Chebyshev error confirming robustness of the proposed filter design. The proposed model reduced computation cost as well as area significantly that affirms computational as well as hardware efficiency. It supports the usefulness of the proposed CPDF FIR filter for real-world filter

applications, especially for speech signal filtering, or denoising, and numerous industrial sensor data filtering and reconstruction.

REFERENCES

1. *S.K. Mitra, Digital Signal Processing: A Computer-based Approach, 2nd ed., McGraw Hill, New York, 2001.*
2. *J.G. Proakis, Digital Signal Processing: Principles, Algorithms, and Applications, Prentice Hall of India, New Delhi, 1997.*
3. *B. Somanathan Nair, Digital Signal Processing: Theory, Analysis and Digitalfilter Design, Prentice-Hall of India, New Delhi, 2004.*
4. *L. Tan, Digital Signal Processing: Fundamentals and Applications, Academic Press, New York, 2011.*
5. *J. Tian, G. Li, Q. Li, Hardware-efficient parallel structures for linear-phase FIR digital filter, in: Proceedings of 56th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2013), 2013, pp. 995–998.*
6. *V. Pavlovic, M. Lutovac, M. Lutovac, Efficient implementation of multiplierless recursive low pass FIR filters using computer algebra system, in: Proceedings of 11th IEEE International Conference on Telecommunication in Modern Satellite, Cable and Broadcasting Services(TELSIKS 2013), Vol. 1, 2013, pp. 65–68.*
7. *W.B. Ye, Y.J. Yu, Single-stage and cascade design of high order multiplier-less linear phase FIR filters using genetic algorithm, IEEE Trans. Circuits Syst. I Regular Pap. 60(11)(2013) 2987–2997.*
8. *C. Xu, S. Yin, Y. Qin, H. Zou, A novel hardware efficient FIR filter for wireless sensor networks, in: Proceedings of Fifth IEEE International Conf. on Ubiquitous and Future Networks(ICUFN 2013), 2013, pp.197–201.*